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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,270	02/20/2001	Olivier F. Prache	43100-06157	2909

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EXAMINER	
SAID, MANSOUR M	
ART UNIT	PAPER NUMBER
2673	9

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,270	PRACHE, OLIVIER F.	
	Examiner	Art Unit	
	MANSOUR M SAID	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1, 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (6,323,836 B1) in view of Kuga (5,828,367).

As to claims 1 and 13, Shin teaches that a display apparatus for displaying input image data, comprising a display generator (clock generator, (figures 7 & 9)), the display generator (controller, (figures 7 & 9)) adapted to provide a display output by employing image data (abstract, column 3, lines 32-63, column 5, lines 28-53 & column 6, lines 67); a buffer (memory, figures 7 & 9, (230)) coupled to the display generator (clock generator, (figures 7 & 9)) the buffer storing image data corresponding to the image data employed by the display generator (abstract, column 5, lines 28-65 & column 6, lines 20-40); and a first data update rate and a second rate (figure 8, (column 5, lines 54-67)), the second rate is lower than the first rate (figure 8, abstract and column 5, lines 54-67)), whereby the power consumption of the display device is reduced by the selective receiving of the input image data (column 3, lines 10-15).

Shin does not disclose that a reception circuit coupled to the image buffer, receiving input image data and update the image data in the buffer.

However, Kuga teaches a reception circuit (control unit, (figure 1, (10)) coupled to the image buffer (driver, (figure 1, (9), receiving input image data and update the image data in the buffer (column 3, lines 10-67).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Kuga's teaching into Shin's system so as to reduce a power consumption without substantial deterioration in the quality of the image displayed (column 1, lines 55-61).

As to claim 4, Kuga teaches that the reception circuit gates the input image databased on occurrences of a vertical synchronization pulse (column 1, lines 28-52, column 4, lines 30-43 and column 6, lines 30-45).

3. Claims 2-3, 5-8, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Kuga as applied to claim 1 above, and further in view of Ilcisin et al. (5,978,052; hereinafter referred to as Ilcisin).

As to claim 2, Shin and Kuga teach all claimed limitation except that an analog storage element, and digital storage element.

However, Ilcisin teach that the buffer is selected from the group consisting of an analog storage element, and digital storage element and both analog and digital storage elements (column 3, lines 49-59 and column 4, lines 1-26).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to have Ilcisin's teaching into Shin's modified device so as to increase the versatility of the device.

As to claims 3 and 5, Shin and Kuga teach all claimed limitation but the input image data in increments of at least one frame/ at least one line from a plurality of input image data frames.

However, Ilcisin teaches that but the input image data in increments of at least one frame/ at least one line from a plurality of input image data frames (abstract, column 3, lines 65-67, column 4, lines 1-67 and column 5, lines 13-27).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to have Ilcisin's teaching into Shin's modified device so as to increase the versatility of the device.

As to claim 6, Ilcisin teaches that a counter for tracking which of said at least one line is to be received (column 5, lines 13-27).

As to claim 7, Ilcisin teaches that input image data in increments of at least one pixel cell (column 4, lines 53-67 and column 5, lines 13-27).

As to claim 8, Ilcisin teaches that a memory array for storing pixel cell data (column 4, lines 53-67).

As to claim 10, Kuga teaches that the memory (memory, (figure 1, (13)) array further comprises an interface controller (storage controller, (figure 1, (12)) (column 3, lines 25-37).

As to claim 11, Kuga teaches that the input image data to memory array elements corresponding to image pixels (figure 1, column 4, lines 30-43).

As to claim12, Kuga teaches that The apparatus of claim 1, wherein the reception circuit is adapted to alternatively receive the input image data at the first rate to provide a substantially real-time video display (figure 1 and column 3, lines 12-67).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Kuga as applied to claim 7 above, and further in view of Arias-Estrada (6,253,161 B1).

Shin and Kuga teach all claimed limitation in claim 9 except that at least one pixel cell comprises a static RAM cell.

However, Arias-Estrada teach that at least one pixel cell comprises a static RAM cell (column 8, lines 18-30).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to have Arias-Estrada's teaching into Shin's modified device so as to increase the versatility of the device.

5. Claims 14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki (6,049,321).

As to claim 14 and 22, Sasaki teaches that a low power display device for displaying input image data (column 1, lines 5-10, column 2, lines 40-45 and column 2, line 66 through column 3, line 1), comprising, a pixel array disposed on the substrate, the pixel array including a plurality of display pixels (column 1, lines 1-30), the pixel array adapted to provide a display output by selectively powering each of the display pixels and by referring to image data corresponding to each of said display pixels (column 1, lines 1-30), a memory module, the memory module storing image data corresponding to each of said display pixels (column 5, lines 53-59), an interface controller adapted to facilitate the directing of image data corresponding to each of the display pixels to a corresponding memory location (figure 1, column 4, lines 4-67 and column 5, lines 53-59) and a sampling circuit adapted to receive input image data , the

sampling circuit selectively storing the input image data so as to sample the input image data at a reduced rate, the sampled image data provided to the driver module (abstract, column 3, lines 7-30, column 8, lines 44-67, column 9, lines 1-25 and column 10, line 62 through column 11, line 11), whereby the driver circuit consumes less power by selectively sampling the input image data (column 1, lines 5-10, column 2, lines 40-45 and column 2, line 66 through column 3, line 1).

Sasaki does not expressly disclose that a silicon substrate.

However, Sasaki discloses that a glass substrate silicon layer covered by a silicon layer (column 7, lines 35-51).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to have a silicon substrate (silicon layer) into Sasaki's system so as to provide a display panel with increased brightness.

6. Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin.

Shin teaches receiving input image data into the display device (column 3, lines 30-67 and column 12-41), the input image data received at a first rate (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40); selectively storing the input image date at a second rate (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40); the second rate is lower than the first rate, and providing the selectively stored data to the display image generation portion of the display device (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40).

Shin does not expressly teach that second rate consumed less power than the storing of the image data at the first rate.

However, Shin fairly teaches that second rate (second clock signal speed) consumed less power than the storing of the image data at the first rate (first clock signal speed) (abstract, column 3, lines 15-63, and column 6, line 64 through column 7, line 9).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invasion was made to have less power into Shin's system so as to achieve the low frequency of the clock signal and the small memory in the controlling circuit, and the high efficiency in panel area usage (column 7, lines 4-9).

7. Claims 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Sasali.

As to claims 16 and 21, Shin teaches that an image output from a display device while reducing power consumption (column 3, lines 15-23), comprising: providing a substrate that includes an array of pixels disposed on the substrate and powering select pixels of the substrate (figures 1-2, and column 1, lines 15-56); receiving input video data, the input video data provided at a first rate device (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40), the second rate lower than the first rate device (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40) and the buffer data employed to selectively power the array of pixels to deliver a video image (figures 1-2, and column 1, lines 15-56).

Shin doss not expressly disclose that sampling the input data with a sampling interface.

However, Sasaki disclose that sampling the input data with a sampling interface (abstract,

column 3, lines 7-30, column 8, lines 44-67, column 9, lines 1-25 and column 10, line 62 through column 11, line 11).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to have a silicon substrate (silicon layer) into Sasaki's system so as to provide a display panel with increased brightness.

8. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilcisin in view of Shin.

As to claims 18 and 21, Ilcisin teaches that a method for reducing power consumption in a video display device, comprising receiving input video data (abstract and column 3, lines 49-67), the input video data corresponding to video image frames (abstract, column 3, lines 49-67, column 4, lines 1-6 and column 4, lines 53-67), selectively updating a frame buffer with received input data (abstract, column 3, lines 49-67, column 4, lines 1-6, column 4, lines 53-67, column 5, lines 127 and column 6, lines 1-36); and displaying an image from the video display device by employing the data stored in the frame buffer (abstract, column 4, lines 1-7, column 4, line 53 through column 5, line 1, and column 5, lines 13-27).

Ilcisin does not teach that the input video data provided at a first frame rate and, the second frame rate is lower than the first frame rate.

However, shin teaches that the input video data provided at a first frame rate (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40), and the second frame rate is lower than the first frame rate (figures 7-10, abstract, column 5, lines 15-67 and column 6, lines 1-40).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to combine Shin's teaching having first and second clock signal speed into Ilcisin's device so as to provide an improved driving circuit for a liquid crystal display that has a low power consumption and a small occupation area (column 3, lines 15-20).

As to claim 19, Ilcisin teaches that the data corresponding to image frame lines are updated at the same rate for all image frame lines (abstract, column 3, lines 6-16, column 4, lines 27-41, and column 5, lines 1-37).

As to claim 20, Ilcisin teaches that the data for a select set of image frame lines are updated at a higher rate than data for the remaining image frame lines (abstract (abstract, column 3, lines 6-16, column 4, lines 27-41, and column 5, lines 1-37).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Mansour M. Said** whose telephone number is **(703) 306-5411**.

The examiner can normally be reached on Monday through Thursday from 8:30 a.m. to 6:00 p.m. The examiner can also be reached on alternate Friday from 8:30 a.m. to 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Shalwala Bipin**, can be reached at **(703) 305-4938**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist)

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer service Office Whose telephone number is (703) 306-0377.

Patent Examiner

August 24, 2003

Mansour M. Said

VIJAY SHANKAR
PRIMARY EXAMINER